IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Qing Ma et al.	Examiner: Sheila V. Clark
Serial No.:	09/640,961	Group Art Unit: 2823
Filed:	August 16, 2000	Docket No.: P9556
Title:	DIRECT BUILD-UP LAYER ON AN ENCAPSULATED DIE PACKAGE	

Customer Number: 59796

APPELLANTS' BRIEF ON APPEAL

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
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Sir:

The Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed April 2, 2010, from the Final Rejection of claims 1-4, 24-29, 21, and 33-40 of the above-identified Application, as set forth in the Final Office Action mailed on February 2, 2010.

Pursuant to 37 C.F.R. 41.37(a), this Appeal Brief is submitted singly. The Commissioner of Patents and Trademarks is hereby authorized to charge Deposit Account No. 50-0221 in the amount of $540.00 which represents the requisite fee set forth in 37 C.F.R. § 41.20(b)(2). The Appellants respectfully request reconsideration and reversal of the Examiner's rejections of the pending claims.

APPELLANTS' BRIEF ON APPEAL

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1. REAL PARTY IN INTEREST1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned Application is the Assignee, Intel Corporation.

2. RELATED APPEALS AND INTERFERENCES2. RELATED APPEALS AND INTERFERENCES

In accordance with 37 CFR §41.37(c)(1)(ii) requiring identification of all other appeals and interferences which would have any bearing on the Board's Decision in the present Appeal, to the best knowledge of Appellant, there have not been and are not any other Appeals, and no Interferences, based on the subject application.

3. STATUS OF THE CLAIMS

In accordance with 37 CFR § 41.37(c)(1)(iii) requiring a statement of the status of all claims, pending and cancelled, Appellant submits the following:

Claims 1-40 have been advanced during prosecution of this Application.

Claims 5-23 have been withdrawn.

Claims 1-4, 24-29, 31, and 33-40 are pending and rejected.

In view of the requirements under 37 CFR §1.191 that an Appeal in an application or reexamination preceding identify, when the Appeal is taken, all rejected claim or claims which are to be appealed and proposed to be contested, Appellant respectfully submits that all presently rejected claims (Claims 1-4, 24-29, 31, and 33-40) are appealed.

4. STATUS OF AMENDMENTS

The following is a statement of the status of any Amendments filed subsequent to final rejection (as required by 37 CFR §41.37(c)(1)(iv)).

No amendments have been made subsequent to the Final Office Action dated February 2, 2010.

5. SUMMARY OF CLAIMED SUBJECT MATTER

A concise explanation of the claimed embodiments defined in the claims in the Appeal, which refers to the specification by page and line number and to the drawings by reference characters (as required by 37 CFR §41.37(c)(1)(v))is detailed as follows.

A claimed embodiment includes a microelectronic package. Reference can be made to FIG. 1f, and to pages 5-8 of the application as filed for illustration of a summarized embodiment.

A microelectronic package, comprising:

a microelectronic die (102) having an active surface (106) and at least one side (116);

encapsulation material (112) adjacent said at least one microelectronic die side (116), wherein said encapsulation material (112) includes at least one surface (110) substantially planar to said microelectronic die (102) active surface (106);

a first dielectric material layer (118) disposed on at least a portion of said microelectronic die (102) active surface (106) and said encapsulation material surface (110); and

at least one first conductive trace (124) disposed on said first dielectric material layer (118) and in physical and electrical contact with said microelectronic die (102) active surface (106), wherein said at least one first conductive trace (124) extends adjacent said microelectronic die (102) active surface (106) and adjacent said encapsulation material surface (110).

6. ISSUES PRESENTED FOR REVIEW

In accordance with 37 CFR §41.37(c)(1)(vi)), the following is a concise statement of each ground of rejection presented for review.

1) Whether claims 1 and 31 are patentable under 35 USC § 102(b) over Fordemwalt et al. (U.S. 3,407,479), where all claim elements are not taught in the reference.

2) Whether claims 1, 4, 24, 26, 27, 31, 35, 36 and 38-40 are patentable under 35 USC § 102(b) over Donovan et al. (U.S. 3,343,255) where Donovan does not teach all claim limitations.

3) Whether Claims 1-3, 25-29, 31-35 and 37-40 are patentable under 35 USC § 103(a) over Chung (U.S. 6,288,905) where all claim limitations are not taught in the single reference.

4) Whether Claims 26 and 27 are patentable under 35 USC § 103(a) over Fordemwalt et al. (U.S. 3,407,479) where all claim limitations are not taught in the single reference.

5) Whether Claims 26 and 27 are patentable under 35 USC § 103(a) over Nishihara et al. (U.S. 6,013,953) where all claim limitations are not taught in the single reference.

6) Whether Claims 4, 24, 35 and 36 are patentable under 35 USC § 103(a) over Chung or Nishihara et al. of Fordemwalt et al. in view of Donovan et al where all claim limitations are not taught, inherently or expressly in the cited references.

7. ARGUMENT

The contentions of Appellant with respect to the issue presented for review in the foregoing Item 6 and the basis therefor, with citations of the authorities, statutes, and parts of the record relied on, (as required by 37 CFR §1.1 92(c)(8)), are provided as follows, with each issue being treated under a separate heading.

For each rejection under 35 USC § 102(b) or (e), Appellant's argument specifies (as required by 37 CFR 41.37(c)(1)(vii)) the errors in the rejection and why the rejected claims are patentable under 35 USC §102(b), including any specific limitations in the rejected claims which are not described in the prior art relied upon in the rejection.

For each rejection under 35 USC § 103(a), Appellant's argument specifies (as required by 37 CFR 41.37(c)(1)(vii)) the errors in the rejection and why the rejected claims are patentable under 35 USC §102(a), including any specific limitations in the rejected claims which are not described in the prior art relied upon in the rejection.

All descriptions of Appellant's disclosed and claimed embodiments, and all descriptions and rebuttal arguments regarding the applied references, as previously submitted by Appellant in any form, are repeated and incorporated herein by reference. Further, all Examiner statements regarding the objections and rejections are respectfully traversed. Further, Appellant submits the following.

A) The Applicable Law

1) §102. Conditions for patentability; novelty and loss of right to patent

A person shall be entitled to a patent unless--

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States

M.P.E.P. §2131, 8th Ed., Rev. 1 Anticipation – Application of 35 U.S.C. § 102(b)
"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (*Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

[A] claim is anticipated only if each and every element as set forth in the claims is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil of California, 814 F.2d 628, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co. 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Further, "the prior art reference must be enabling, thus placing the allegedly disclosed matter in the possession of the public." In re Brown, 141 USPQ 245, 249 (CCPA 1964). In particular, Brown repeats old law (1890) that

> the description must place the invention in the possession of the public as fully as if the art or instrument itself had been practically and publicly employed. In order to accomplish this it must be so particular and definite that from it alone, without experiment or the exertion of his own inventive skill, any person versed in the art to which it appertains could construct and use it.

Id. at 249.

2) M.P.E.P. § 2173.01 Claim terminology

A fundamental principle contained in 35 U.S.C. 112, second paragraph is that Appellants are their own lexicographers. They can define in the claims what they regard as their invention essentially in whatever terms they choose so long as any special meaning assigned to a term is clearly set forth in the specification … a claim may not be rejected solely because of the type of language used to define the subject matter for which patent protection is sought.

M.P.E.P. § 2111.01 Plain meaning
[T]he words of the claim must be given their plain meaning unless Appellant has provided a clear definition in the specification. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

M.P.E.P. § 2111.01
"[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application."
Phillips v. AWH Corp., *>415 F.3d 1303, 1313<, 75 USPQ2d 1321>, 1326<
(Fed. Cir. 2005) (en banc).

3). **§ 103. Conditions for patentability; non-obvious subject matter**

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject

matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

B Argument

B1) Claims 1 and 31 are patentable under 35 USC § 102(b) over Fordemwalt et al. (U.S. 3,407,479), because all claim elements are not taught in the reference.

Claim 1 requires "at least one first conductive trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface. . . ." Claim 1 requires the conductive trace extend adjacent the die side as well as adjacent the encapsulation material. Fordemwalt does not show a die side, as he illustrates "islands" (e.g. column 2, line 47) in a single wafer with "cut-away" edges that are indeterminate as to where the die side is. It therefore cannot be ascertained whether Fordemwalt teaches a conductive trace to extend adjacent the die side. Consequently, Fordemwalt does not teach or enable what is claimed.

Regarding claim 1, Fordemwalt's connector fails to teach a limitation of claim 1, "wherein said at least one first conductive trace extends adjacent said microelectronic die active surface". Fordemwalt also fails to teach a limitation of claim 1, "wherein said at least one first conductive trace extends . . . adjacent said encapsulation material surface".

Regarding claim 31, Fordemwalt fails to teach at least the limitation "wherein said at least one conductive trace extends adjacent said microelectronic die active surface". Each and every element is not found, either expressly or inherently described, in Fordemwalt.

B2) Claims 1, 4, 24, 26, 27, 31, 35, 36 and 38-40 are patentable under 35 USC § 102(b) over Donovan et al. (U.S. 3,343,255) because Donovan does not teach all claim limitations.

Considerable effort has been expended by the Examiner to define a trace. Most of this effort has been *ad hoc* definitions. The Appellant has provided a standard reference: Harper: "Electronic Packaging and Interconnection Handbook" (3rd Ed., McGraw–Hill 2000) to demonstrate the meaning of a trace. The Appellant contends that the ordinary and customary meaning of the claim term "trace" is the meaning that the term would have to a person of

ordinary skill in the art as defined and demonstrated in Harper. The Examiner has not objected to this standard reference. Absent refutation by the Examiner of Harper's meaning of trace, the Appellant contends none of the cited references teach or suggest the scope of what is claimed.

Claim 1 has the limitation of "wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface". This limitation is not taught in Donovan. The Examiner incorrectly refers to a "trace 32" that is an "ohmic contact 32". The ohmic contact 32 is not a trace as taught, claimed, and understood by persons of ordinary skill in the art. The ohmic contact 32 also does not have the structural limitation of "wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface" as claimed. Each and every element of claim 1 is not taught by Donovan.

Claims 4 and 24 depend from claim 1 and are therefore not anticipated. Further, Donovan fails to teach the limitation of claim 24, particularly the limitation the "said encapsulation material is adjacent at least a portion of said at least one heat dissipation device." The Examiner previously admitted this deficiency in Donovan.

Regarding claim 26, Donovan fails to teach the limitation "encapsulation material includes . . . at least one surface planar to said microelectronic die back surface." Claims 27 and 30 depend from claim 26, claims 27 and 30 are also not anticipated.

Regarding claim 31, Donovan fails to teach at least the limitation, "at least one first conductive trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface". Donovan also fails to teach at least the limitation "wherein said at least one first conductive trace extends adjacent said microelectronic die active surface". Claims 32, 35, and 36 depend from claim 31 and are not anticipated. Regarding claim 38, Donovan fails to teach at least the limitation, "at least one first conductive trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface". Donovan also fails to teach at least the limitation "wherein said at least one first conductive trace extends adjacent said microelectronic die active

surface". Each and every element is not found, either expressly or inherently described, in Donavan.

B3) Claims 1-3, 25-29, 31-35 and 37-40 are patentable under 35 USC § 103(a) over Chung (U.S. 6,288,905) because all claim limitations are not taught in the single reference.

Claim 1 defines the trace being both physically and electrically in contact with the "microelectronic die active surface". Claim 1 requires "at least one first conductive trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface . . . ." The Examiner calls out Chung's bump 144 to be a trace as claimed. The Appellant contends Chung's "bump 144" cannot be construed as a trace as it is understood by persons of ordinary skill in the art. Because no structure in Chung meets the limitations of claim 1, all the claim limitations are not taught in Chung.

Claims 2-4 and 25 depend from claim 1. Because all the claim limitations are not taught in Chung the rejection fails to establish a *prima facie* case of obviousness. Regarding independent claim 26 and dependent claims 27-29, the Examiner is again using incorrect definitions of a trace. The Appellant has demonstrated these definitions are incorrect.

In previous Office Actions, the Examiner called out Chung's structure 120 as the "first dielectric material layer" that is claimed. But Chung's trace (metal layer 100) is "disposed on said first dielectric material layer" as claimed. The Examiner has asserted several structures in composite are a "trace". But Chung's trace 110 is not "in physical and electrical contact" Chung's active surface. Several intervening structures are between Chung's trace 110 and Chung's active surface.

Chung's trace 110 is in physical contact with Chung's "via conductor 132b" and not with the active surface. The Appellant contends Chung's "via conductor 132b" cannot be construed as a trace as it is understood by persons of ordinary skill in the art. Further, Chung's via conductor 132b is in physical contact with Chung's "oxidation-resistant material 134b" and not with the active surface. The Appellant contends Chung's "oxidation-resistant material 134b" cannot be construed as a trace as it is understood by persons of ordinary skill in the art. Even further, Chung's oxidation-resistant material 134b is in physical contact with Chung's "bump

144" and not with the active surface. The Appellant contends Chung's "bump 144" cannot be construed as a trace as it is understood by persons of ordinary skill in the art. It is only Chung's bump 144 that is in physical contact with Chung's active surface at the "contact pad 142b".

The Appellant respectfully asserts the "first conductive trace" is a single structure with no junctions, as supported by the specification, and as supported by the definition provided by the Examiner in a previous Office Action. Further, previously submitted selected sections of Harper: "Electronic Packaging and Interconnection Handbook" (3rd Ed., McGraw –Hill 2000) are submitted to support Appellant's assertion that a "trace" is a well-known structure and it is distinct from Chung's "via conductor 132b", Chung's "oxidation-resistant material 134b", Chung's "bump 144", and Chung's "contact pad 142b". Particular attention may be drawn to the selected sections taken from Harper. For example, in Section 14.2.1.3, Harper structurally distinguishes a trace from a bond finger, a filled via, a wire, and a solder ball. Chung makes similar distinctions, particularly at least with a bump, a via, and a contact pad.

In Section 14.2.2.1, Harper structurally distinguishes a trace from a wire bond, a via, and a solder ball. These he characterizes as "cylindrical linear elements", and traces as "rectangular linear elements". Harper considers a trace not only different from one of these structures but structurally different from all of them. Chung makes similar distinctions, particularly at least with a bump, a via, and a contact pad.

In Section 14.2.2.4, Harper structurally distinguishes a trace in accordance with the definition provided by the Examiner. Figure 14.10 shows traces, to quote from the definition, "*on the surface* of or *sandwiched* inside a PCB, printed circuit board" (see "Computer, Telephony & Electronics Industry Glossary" http://www.csgnetwork.com/glossaryt.html), as cited to by the Examiner. In every instance where Harper refers to a "trace" his reference is consonant with Appellant's disclosure as taught and claimed. There is no instance where Harper's teaching of a trace that can be construed to be any of Chung's "via conductor 132b", "oxidation-resistant material 134b", Chung's "bump 144", and Chung's "contact pad 142b". Harper has demonstrated that a trace is understood by persons of ordinary skill in the art as a distinct structure that should not be aggregated with other structures such as via conductors, bumps, and pads among other non-trace structures.

Regarding claim 26, claim 30 was added in all limitations to claim 26. Chung fails to teach these limitations. Claims 27-29 depend from claim 26. Regarding claim 31, for reasons similarly to those set forth for claim 1, above, Chung does not teach every element of claim 31. Regarding claim 38, Chung does not teach every element of claim 38.

B4) Claims 26 and 27 are patentable under 35 USC § 103(a) over Fordemwalt et al. (U.S. 3,407,479) because all claim limitations are not taught in the single reference.

The Appellant has demonstrated that Fordemwalt does not show a die side, as he illustrates "islands" (e.g. column 2, line 47) in a single wafer with cut-away edges that are indeterminate as to a die side. Consequently, Fordemwalt does not teach or enable what is claimed.

B5) Claims 26 and 27 are patentable under 35 USC § 103(a) over Nishihara et al. (U.S. 6,013,953) because all claim limitations are not taught in the single reference.

The Examiner states Nishihara has a trace 2 in physical and electrical contact with said microeletronic die active surface. But it is the bond pad 9 and not the trace 2 that is in physical contact with Nishihara's die active surface. All limitations are not taught in Nishinara.

The other limitations cited by the Examiner may describe what is disclosed in Nishihara et al., but claim 1 requires "at least one first conductive trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface . . . ." Nishihara's trace (copper through-hole 5) is not disposed on the first dielectric material (adhesive 3) which is on the active surface of the chip 1. Consequently, the limitation of a first dielectric on the active surface and the trace on the first dielectric is not met in Nishihara.

Nishihara's trace is not in physical contact with the active surface, rather with a "connection terminal 9" that is prominent from the active surface. Each and every element as set forth in claim 1 is not found, either expressly or inherently described, in Nishihara et al. Regarding claim 26, Nishihara fails to teach the limitation "encapsulation material includes. . . at least one surface planar to said microelectronic die back surface." Each and every element of claim 26 is not taught by Nishihara et al. Claim 27 depends from claim 26.

B6) Claims 4, 24, 35 and 36 are patentable under 35 USC § 103(a) over Chung or Nishihara et al. of Fordemwalt et al. in view of Donovan et al because all claim limitations are not taught, inherently or expressly in the cited references.

None of the references alone or in combination teach a trace as claimed and as understood by persons of ordinary skill in the art. The Examiner admits that Chung or Nishihara or Fordemwalt do not teach a heat dissipation device. However, what teaching Donovan et al. adds to teach a heat dissipation device, does not amount to a teaching or suggestion of all the limitations of claims 4, 24, 35, and 36. Further, where heat dissipation (or heat dissipation at all, for that matter) is not mentioned in Chung and/or Donovan et al., the Examiner has used the Appellants' disclosure as a guide to make the claimed combination. Withdrawal of the rejections is respectfully requested.

CONCLUSION

Appellant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Appellant's attorney at (503) 712-3485 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-0221.

Respectfully submitted,

QING MA ET AL.

By their Representatives,
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By /John N. Greaves, Reg. No. 40,362/
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APPENDIX – CLAIMS ON APPEAL

1. A microelectronic package, comprising:

a microelectronic die having an active surface and at least one side;

encapsulation material adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one surface substantially planar to said microelectronic die active surface;

a first dielectric material layer disposed on at least a portion of said microelectronic die active surface and said encapsulation material surface; and

at least one first conductive trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

2. The microelectronic package of claim 1, further including at least one second dielectric material layer disposed over said at least one first conductive trace and said first dielectric material layer.

3. The microelectronic package of claim 2, wherein at least a portion of at least one second conductive trace extends through and resides on said at least one second dielectric material layer.

4. The microelectronic package of claim 1, wherein said microelectronic die further includes a back surface; and further including at least one heat dissipation device in thermal contact with said microelectronic die back surface.

24. The microelectronic package of claim 4, wherein said encapsulation material is adjacent at least a portion of said at least one heat dissipation device.

25. The microelectronic package of claim 1, wherein said microelectronic die further includes a back surface; and wherein at least one surface of said encapsulation material is substantially planar to said microelectronic die.

26. A microelectronic package, comprising:

a microelectronic die having an active surface, a back surface, and at least one side;

encapsulation material adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one surface substantially planar to said microelectronic die active surface and at least one surface planar to said microelectronic die back surface; and

at least one heat dissipation device in thermal contact with said microelectronic die back surface.

27. The microelectronic package of claim 26, further including at least one first conductive trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

28. The microelectronic package of claim 27, further including at least one second dielectric material layer disposed over said at least one first conductive trace and said first dielectric material layer.

29. The microelectronic package of claim 28, wherein at least a portion of at least one second conductive trace extends through and resides on said at least one second dielectric material layer.

31. A microelectronic package, comprising:

a plurality of microelectronic dice each having an active surface and at least one side;

encapsulation material adjacent said at least one microelectronic die side of said plurality of microelectronic dice, wherein said encapsulation material includes at least one surface substantially planar to said plurality of microelectronic dice active surfaces; and

at least one first conductive trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

33. The microelectronic package of claim 31, further including at least one second dielectric material layer disposed over said at least one first conductive trace and said first dielectric material layer.

34. The microelectronic package of claim 33, wherein at least a portion of at least one second conductive trace extends through and resides on said at least one second dielectric material layer.

35. The microelectronic package of claim 31, wherein said microelectronic die further includes a back surface; and further including at least one heat dissipation device in thermal contact with said microelectronic die back surface.

36. The microelectronic package of claim 35, wherein said encapsulation material is adjacent at least a portion of said at least one heat dissipation device.

37. The microelectronic package of claim 31, wherein said microelectronic die further includes a back surface; and wherein at least one surface of said encapsulation material is substantially planar to said microelectronic die active surface.

38. A microelectronic package, comprising:

a microelectronic die having an active surface, a back surface, and at least one side; encapsulation material adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one surface substantially planar to said microelectronic die active surface;

a first dielectric material layer disposed on at least a portion of said microelectronic die active surface and said encapsulation material surface;

at least one first conductive trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface; and

at least one heat dissipation device in thermal contact with said microelectronic die back surface.

39. The microelectronic package of claim 38, further including:

at least one second dielectric material layer disposed over said at least one first conductive trace and said first dielectric material layer, wherein at least a portion of at least one second conductive trace extends through and resides on said at least one second dielectric material layer.

40. The microelectronic package of claim 39, wherein said encapsulation material is adjacent at least a portion of said at least one heat dissipation device.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

No Related Proceedings are known to the Appellants' Representative.